Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (Original) A power amplifier, comprising:

an amplifying transistor;

a bias circuit including a bias transistor, the bias circuit providing a bias current to bias the amplifying transistor; and

a bias current control circuit, responsive to fluctuation in a reference voltage and variation in temperature, for adjusting the bias current to control an operation current in the amplifying transistor.

2. (Original) The power amplifier of claim 1, wherein the bias circuit further includes a first resistor having a first and a second end thereof, the first end being supplied with the reference voltage and the second end being connected to a base of the bias transistor.

3. (Original) The power amplifier of claim 2, wherein the bias current control circuit includes:

a first diode having a cathode and an anode thereof, the first diode being made of a bipolar junction transistor, whose collector and base are connected to each other;

a second diode having a cathode and an anode thereof, the second diode being made of a bipolar junction transistor whose collector and base are connected to each other, the cathode of the second diode being grounded, and the anode of the second diode being connected to the cathode of the first diode;

a second resistor having a first and a second end thereof, the first end of the second resistor being supplied with the reference voltage and the second end of the second resistor being connected to the anode of the first diode; and

a control transistor, an emitter thereof being grounded and a base thereof being connected to the anode of the second diode and a collector thereof being connected to a node P between the second end of the first resistor and the base of the bias transistor.

4. (Original) The power amplifier of claim 3, wherein, if the reference voltage increases, a collector current of the control transistor increases, and, if otherwise, the collector current of the control transistor decreases to thereby maintain a voltage Vp at the node P substantially constant.

5. (Original) The power amplifier of claim 3, wherein, if temperature rises, a collector current of the control transistor increases, and, if otherwise, the collector current of the control transistor decreases to thereby compensate fluctuations in a voltage Vp at the node P.

6. (Original) The power amplifier of claim 4, wherein a voltage fluctuation ΔVp at the node P can be calculated as follows:

$$\Delta Vp = V'p - Vp \cong \pm \Delta Vref \mp \Delta Vref \frac{R2}{R1},$$

wherein the V'p is a voltage at the node P when the reference voltage is fluctuated, the $\Delta Vref$ is a fluctuation in the reference voltage, R1 is the second resistor and R2 is the first resistor.

7. (Original) The power amplifier of claim 5, wherein a voltage fluctuation ΔVp at the node P can be calculated as follows:

$$\Delta Vp \cong \mp(\Delta V_{BE1} + \Delta V_{BE2})\frac{R2}{R1},$$

wherein the ΔV_{BE1} is a turn-on voltage fluctuation in the amplifying transistor, ΔV_{BE2} is a turn-on voltage fluctuation in the bias transistor, R1 is the second resistor and R2 is the first resistor.

8. (New) A power amplifier, comprising:

an amplifying transistor;

a bias circuit including a bias transistor, the bias circuit providing a bias current to bias the amplifying transistor; and

a bias current control circuit, regardless of fluctuation in a reference voltage and variation in temperature, for maintaining an operation current in the amplifying transistor at a constant level by controlling a base voltage of the bias transistor.

9. (New) The power amplifier of claim 8, wherein the bias circuit further includes a first resistor having a first and a second end thereof, the first end being supplied with the reference voltage and the second end being connected to a base of the bias transistor.

10. (New) The power amplifier of claim 9, wherein the bias current control circuit includes:

a first diode having a cathode and an anode thereof, the first diode being made of a bipolar junction transistor, whose collector and base are connected to each other;

a second diode having a cathode and an anode thereof, the second diode being made of a bipolar junction transistor whose collector and base are connected to each other, the cathode of the second diode being grounded, and the anode of the second diode being connected to the cathode of the first diode;

a second resistor having a first and a second end thereof, the first end of the second resistor being supplied with the reference voltage and the second end of the second resistor being connected to the anode of the first diode; and

a control transistor, an emitter thereof being grounded and a base thereof being connected to the anode of the second diode and a collector thereof being connected to a node P between the second end of the first resistor and the base of the bias transistor.

11. (New) The power amplifier of claim 10, wherein, if the reference voltage increases, a collector current of the control transistor increases, and, if otherwise, the collector current of the control transistor decreases to thereby maintain a voltage Vp at the node P substantially constant.

12. (New) The power amplifier of claim 10, wherein, if temperature rises, a collector current of the control transistor increases, and, if otherwise, the collector current of the

control transistor decreases to thereby compensate fluctuations in a voltage Vp at the node P.

13. (New) The power amplifier of claim 11, wherein a voltage fluctuation ΔVp at the node P can be calculated as follows:

$$\Delta Vp = V'p - Vp \cong \pm \Delta Vref \mp \Delta Vref \frac{R2}{R1},$$

wherein the V'p is a voltage at the node P when the reference voltage is fluctuated, the $\Delta Vref$ is a fluctuation in the reference voltage, R1 is the second resistor and R2 is the first resistor.

14. (New) The power amplifier of claim 12, wherein a voltage fluctuation ΔVp at the node P can be calculated as follows:

$$\Delta Vp \cong \mp(\Delta V_{BE1} + \Delta V_{BE2})\frac{R2}{R1},$$

wherein the ΔV_{BE1} is a turn-on voltage fluctuation in the amplifying transistor, ΔV_{BE2} is a turn-on voltage fluctuation in the bias transistor, R1 is the second resistor and R2 is the first resistor.